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NETTUR TECHNICAL TRAINING FOUNDATION

DIPLOMA IN ELECTRONICS ENGINEERING & EMBEDDED SYSTEM – CP04

V SEMESTER REGULAR & SUPPLEMENTARY EXAMINATION-JAN 2023

Subject: VLSI Technology **Total Time: 2 Hr.**
Subject Code: CP04503T **Total Marks: 50 Marks**

PART B

1.0 ANSWER ANY EIGHT OF THE FOLLOWING **2*8=16**

1.1 State Moore's Law
1.2 Explain right shift and left shift operator in Verilog
1.3 Write the rules for naming an identifiers or user defined words in Verilog
1.4 Write a short notes on Sensitivity list
1.5 List out the different port modes in Verilog
1.6 What is Recurring cost?
1.7 What are the different levels in which testing a chip or die can occur?
1.8 What is ATPG?
1.9 Write the expansion of a) HDL b) EDA
1.10 List out the binary values supported by Verilog

2.0 ANSWER ANY SIX OF THE FOLLOWING **3*6=18**

2.1 Write the classifications of Integrated Circuit
2.2 List out the data types available in Verilog
2.3 Explain the Relational operators in Verilog with example
2.4 Write the syntax for if else statement in Verilog
2.5 Write a Verilog program to implement OR gate
2.6 Explain 2 input NAND gate CMOS circuit
2.7 What is PLA and how it is supporting to design
2.8 What is prototype cost?

3.0 ANSWER ANY FOUR OF THE FOLLOWING **4*4=16**

3.1 Write the differences between FPGA and CPLD
3.2 List out the types of MOSFET's and explain its working
3.3 Explain any 2 of the following 1. IDDQ Test 2.BIST 3. Design for Manufacturability
3.4 Explain VLSI design flow
3.5 Explain the four structured design techniques used in design of IC
3.6 Explain what is meant by Struck-at-1 fault and Struck-at-0 fault