

NETTUR TECHNICAL TRAINING FOUNDATION DIPLOMA IN MECHATRONICS ENGINEERING & SMART FACTORY-CP15 III SEMESTER REGULAR & SUPPLEMENTARY EXAMINATION-JAN 2023

Subject: Digital Electronics Subject Code: CP15301T	Total Time: 2 Hr. Total Marks: 50 Marks
PART H	3
1.0 ANSWER ANY EIGHT OF THE FOLLO	WING 2*8=16
1.1 Define the following terms related to pulse w	aveforms
a)Frequency b)Time Period	
1.2 How many no. of bits, nibbles, bytes are ther	e in the given binary data (1011 0101)?
1.3 What are universal gates why are they called so	o?
1.4 List the rules of Boolean algebra	
1.5 Draw the logic symbol and truth table for Ha	lf Adder
1.6 Define Multiplexer. Draw the block diagram	of Multiplexer.
1.7 Differentiate between Flip-flop & Latches.	
1.8 Define Modulus of Counters.	
1.9 Define Data Conversion. List the types of Da	ta Converters.
1.10 What are the different names of Johnson Co	ounter?
2.0 ANSWER ANY SIX OF THE FOLLOWI	NG 3*6=18
2.1 E_{-1}	next discuss

- 2.1 Explain the working of BJT as a switch with neat diagram
- 2.2 Convert the given BCD number (0011 0001) to Binary number
- 2.3 Classify the logic gates.
- 2.4 Minimize the given 3-variable SoP expression using K Map

 $Y = A\bar{B}C + \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}\bar{C} + \bar{A}\bar{B}\bar{C}$

4*4=16

- 2.5 Draw the logic circuit for 1-bit Comparator & write the truth table for the same
- 2.6 Define Multivibrator. List the modes of operation of IC 555 Timer
- 2.7 Define triggering & what are the types of triggering?
- 2.8 Differentiate between Binary Weighted DAC & R-2R Ladder DAC.

3.0 ANSWER ANY FOUR OF THE FOLLOWING

- 3.1 Differentiate between Asynchronous Counters & Synchronous Counters
- 3.2 Explain the working of MOD-10 Ripple Up Counter
- 3.3 Explain the working of successive approximation type of ADC with neat sketch
- 3.4 Draw the logic circuit for CMOS based NAND & NOR Logic Gates.
- 3.5 Explain the working of 4-bit SISO Shift Register with neat diagram.
- 3.6 Explain how JK Flip-flop is converted into T Flip-flop

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